UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,433	03/31/2004	Simon Knowles	66365-021	3801

7590 12/12/2006

MCDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
FIEGLE, RYAN PAUL	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,433	KNOWLES, SIMON	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The examiner notes with appreciation and accepts the new title.

Claim Rejections - 35 USC § 101

2. The examiner notes with appreciation and accepts the amendments to the claims to remedy the 101 issues.

Claim Rejections - 35 USC § 112

3. Applicant's arguments, see paragraph 4 of page 10, filed 9/22/06, with respect to claims 1-23 have been fully considered and are persuasive. The rejection of claims 1-23 with respect to the 112 issues has been withdrawn.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger (US Patent 5,737,631) in view of Johnson (US Patent 5,136,697).

6. As per claim 1:

A computer processor having control and data processing capabilities comprising:

a decode unit for decoding instructions (Trimberger: Figure 2, item 112);

a data processing facility comprising a first data execution path including fixed operators (Trimberger: Figure 2, item 100) and a second data execution path including at least configurable operators (Trimberger: Figure 2, item 120), said configurable operators having a plurality of predefined configurations, at least some of which are selectable by means of an opcode portion of a data processing instruction (Trimberger: column 2, lines 62-67; column 3, lines 1-9; Figure 3, item 201);

wherein said decode unit is operable to detect whether a data processing instruction defines a fixed data processing operation or a configurable data processing operation, said decode unit causing the computer system to supply data for processing to said first data execution path when a fixed data processing instruction is detected and to said configurable data execution path when a configurable data processing instruction is detected (Trimberger: column 7, lines 45-50).

Trimberger does not teach a control processing facility comprising a control execution path.

Program control flow execution units, i.e. branching execution units; and their benefits are well documented in the art.

Johnson teaches a branching execution unit (Johnson: Figure 7, item 22) that is able to reduce the processing delays associated with branching instructions (Johnson: column 1, lines 9-11) in conjunction with cache entries that contain branch prediction

information (Johnson: column 2, lines 55-66). The dedicated branching execution unit is pinnacle to the function of the Johnson's branch prediction scheme (Johnson: column 7, lines 3-63).

It would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Johnson's dedicated branching execution unit to Trimberger would reduce the processing delays associated with branching instructions.

7. As per claim 2:

A computer processor according to claim 1, wherein the decode unit is capable of decoding a stream of instruction packets from memory, each packet comprising a plurality of instructions (Trimberger: column 7, lines 51-56).

8. As per claim 3:

A computer processor according to claim 1, wherein the decode unit is operable to detect if an instruction packet contains a data processing instruction (Trimberger: column 7, lines 45-50).

9. As per claim 4:

A computer processor according to claim 1, wherein the configurable operators are configurable at the level of multibit values (Trimberger: column 9, lines 18-19) (The opcode is a multibit value).

10. As per claim 5:

A computer processor according to claim 4, wherein the configurable operators are configurable at the level of multibit values comprising four or more bits (Trimberger: column 9, lines 18-19) (The opcode is at least 4 bits).

11. As per claim 6:

A computer system according to claim 4, wherein the configurable operators are configurable at the level of words (Trimberger: column 9, lines 24-25) (Immediate values are optional; therefore, the whole word is configurable).

12. As per claims 7 and 8:

Official notice is taken that, while Trimberger does not state that his FXUs are SIMD, such would have been obvious to one of ordinary skill in the pertinent art since the advantages and implementations of SIMD are well known.

13. As per claim 9:

A computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the nature of the operations performed (Trimberger: column 8, lines 5-17).

14. As per claim 10:

A computer processor according to claim 9, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the nature of the operations performed from a field of an instruction defining a configurable data processing operation (Trimberger: column 7, lines 62-67; column 8, lines 1-17).

15. As per claim 11:

A computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive configuration information comprising information controlling relative interconnectivity (Trimberger: column 8, lines 35-37).

16. As per claim 12:

A computer processor according to any of claim 9, comprising a control map associated with configurable operators of the second data execution path, said control map being operable to receive at least one configuration bit from a configurable data processing instruction and to provide configuration information to the configurable operators responsive thereto (Trimberger: column 7, lines 62-67; column 8, lines 1-17).

17. As per claim 13:

A computer processor according to claim 12, wherein said configuration information controls interconnectivity between two or more of said configurable operators (Trimberger: column 8, lines 35-37).

18. As per claim 14:

A computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive either configuration information determining the nature of an operation to be performed or configuration information controlling interconnectivity from a source other than a configurable data processing instruction (Trimberger: column 8, lines 5-17; Figure 2; items 101, 102 and 123).

19. As per claim 15:

A computer processor according to claim 1, wherein at least one configurable operator of the second data execution path is capable of executing data processing

instructions with an execution depth greater than two computations before returning results to a results store (Trimberger: column 3, lines 10-27) (It is inherent that these complex functions will take at least two cycles).

20. As per claim 16:

A computer processor according to claim 1, comprising a switch mechanism for receiving data processing operands from a configurable data processing instruction and switching them as appropriate for supply to one or more of said configurable operators (Trimberger: column 7, lines 45-50).

21. As per claim 17:

A computer processor according to claim 1, comprising a switch mechanism for receiving results from one or more of said configurable operators and switching the results as appropriate for supply to one or more of a result store and feed back loop (Trimberger: column 8, lines 51-59).

22. As per claim 18:

A computer processor according to claim 1, comprising a plurality of control maps for mapping configuration bits received from configurable data processing instructions to configuration information for supply to configurable operators of the second data execution path (Trimberger: column 3, lines 66-67; column 4, lines 1-10).

23. As per claim 19:

A computer processor according to claim 1, comprising a switch mechanism for receiving configuration information from a control map and switching it as appropriate

for supply to configurable operators of the second data execution path (Trimberger: column 8, lines 5-17).

24. As per claim 20:

A computer processor according to claim 1, comprising configurable operators selected from one or more of: multiply accumulate operators; arithmetic operators; state operators; and cross-lane permuters (Trimberger: column 3, lines 10-27).

25. As per claim 21:

A computer processor according to claim 1, comprising operators and an instruction set capable of performing one or more operations selected from: Fast Fourier Transforms; Inverse Fast Fourier Transforms; Viterbi encoding/decoding; Turbo encoding/decoding; and Finite Impulse Response calculations; and any other Correlations or Convolutions (Trimberger: column 3, lines 10-27) (polynomial evaluation is used in FFT and IFFT).

26. As per claim 22:

A method of operating a computer processor having control and data processing capabilities, said computer processor comprising a first data execution path including fixed operators and a second data execution path including configurable operators, said configurable operators having a plurality of predefined configurations, at least some of which are selectable by means of an opcode portion of a data processing instruction (Trimberger: column 2, lines 62-67; column 3, lines 1-9), the method comprising:

decoding a plurality of instructions to detect whether at least one data processing instruction, of said plurality of instructions, defines a fixed data processing operation or a configurable data processing operation (Trimberger: column 7, lines 45-50);

causing the computer processor to supply data for processing to said first data execution path when a fixed data processing instruction is detected and to said configurable data execution path when a configurable data processing instruction is detected; and outputting the results (Trimberger: column 7, lines 45-50).

Trimberger does not teach a control execution path.

Program control flow execution units, i.e. branching execution units, and their benefits are well documented in the art.

Johnson teaches a branching execution unit (Johnson: Figure 7, item 22) that is able to reduce the processing delays associated with branching instructions (Johnson: column 1, lines 9-11) in conjunction with cache entries that contain branch prediction information (Johnson: column 2, lines 55-66). The dedicated branching execution unit is pinnacle to the function of the Johnson's branch prediction scheme (Johnson: column 7, lines 3-63).

It would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Johnson's dedicated branching execution unit to Trimberger would reduce the processing delays associated with branching instructions.

27. As per claim 23:

A computer program product comprising program code means for causing a computer processor, said computer processor comprising a first data execution path including fixed operators and a second data execution path, including configurable operators, said configurable operators having a plurality of predefined configurations, at least some of which are selectable by means of an opcode portion of a data processing instruction (Trimberger: column 2, lines 62-67; column 3, lines 1-9), to:

decode a plurality of instructions to detect whether at least one data processing instruction, of said plurality of instructions, defines a fixed data processing operation or a configurable data processing operation (Trimberger: column 7, lines 45-50);

cause the computer processor to supply data for processing to said first data execution path when a fixed data processing instruction is detected and to said configurable data execution path when a configurable data processing instruction is detected; and output the results (Trimberger: column 7, lines 45-50).

Trimberger does not teach a control execution path.

Program control flow execution units, i.e. branching execution units, and their benefits are well documented in the art.

Johnson teaches a branching execution unit (Johnson: Figure 7, item 22) that is able to reduce the processing delays associated with branching instructions (Johnson: column 1, lines 9-11) in conjunction with cache entries that contain branch prediction information (Johnson: column 2, lines 55-66). The dedicated branching execution unit is pinnacle to the function of the Johnson's branch prediction scheme (Johnson: column 7, lines 3-63).

It would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Johnson's dedicated branching execution unit to Trimberger would reduce the processing delays associated with branching instructions.

28. As per claim 24:

A data processing instruction set comprising a first plurality instructions having a field indicating a fixed type of data processing operation and a second plurality of instructions having a field indicating a configurable type of data processing operations (Trimberger: column 9, lines 4-18).

Trimberger does not teach a control execution path.

Program control flow execution units, i.e. branching execution units, and their benefits are well documented in the art.

Johnson teaches a branching execution unit (Johnson: Figure 7, item 22) that is able to reduce the processing delays associated with branching instructions (Johnson: column 1, lines 9-11) in conjunction with cache entries that contain branch prediction information (Johnson: column 2, lines 55-66). The dedicated branching execution unit is pinnacle to the function of the Johnson's branch prediction scheme (Johnson: column 7, lines 3-63).

It would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Johnson's dedicated branching execution unit to Trimberger would reduce the processing delays associated with branching instructions.

It is inherent that the control instructions (branch instruction) also have their own unique opcodes.

29. As per claim 25:

A computer processor having a data execution path comprising configurable operators, wherein the configurable operators comprise a plurality of pro-defined groups of operator configurations, each group comprising operators from a separate operator class (Trimberger: column 2, lines 62-67; column 3, lines 1-27).

Trimberger does not explicitly teach a look-up table to convert relatively bits in an instruction into a set of relatively complex configuration settings for said configurable operators.

Trimberger teaches that the function specified by the configurable operator is kept in the "immediate" field 261 (Trimberger: column 9, lines 38-39). Based on the contents of this field, the operands are routed to the reconfigurable logic to complete the function. With regular, fixed functions, the decoding and routing for an operator is done in one of two ways – 1. hardwiring, or 2. a lookup table. Based on the contents of the lookup table, the decoder knows where to routes operands. With configurable operators, it is impossible to have the routing hardwired since the routing is not known at the time of design. Therefore, a lookup table is necessary.

Therefore, though Trimberger does not explicitly teach a look-up table to convert relatively bits in an instruction into a set of relatively complex configuration settings for said configurable operators, the examiner takes official notice that such would have

been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention since it is a viable solution to route configurable operators in a processor.

30. As per claim 26:

A computer processor according to claim 25, wherein the operator classes comprise classes selected from one or more of: multiply accumulate operators; arithmetic operators; state operators; and permuters (Trimberger: column 3, lines 10-27).

31. As per claim 27:

A computer processor according to claim 25, wherein connections between operators selected from within each of the pre-defined groups of operator configurations are capable of being configured by an opcode portion within an instruction executed by the computer processor (Trimberger: column 2, lines 62-67; column 3, lines 1-9; Figure 3, item 201).

32. As per claim 28:

A computer processor according to claim 25, wherein connections between operators selected from more than one of the pre-defined groups of operator configurations are capable of being configured by an opcode portion within an instruction executed by the computer processor.

While not explicitly stated, such is inherent since the functions defined by Trimberger have overlapping logic (e.g. searching in a document and spell checking will have much of the same logic). Redundant logic on a large function is wasteful.

Therefore, the bitmaps are broken up into smaller functions which can be shared by larger functions.

Response to Arguments

33. Applicant's arguments with respect to claims 1 and 22-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan P Fiegle
Examiner
Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100